TITLE OF THE INVENTION

NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD THEREFOR

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the benefit of priority from the prior Japanese Patent Applications No. 11-073074, filed March 18, 1999; and No. 11-185118, filed June 30, 1999, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

The present invention relates to a nonvolatile semiconductor memory device including stack-gate memory cells each having a control gate electrode and a floating gate electrode and peripheral circuits of the memory cells which are integrated on one chip and a manufacturing method therefor. More particularly, the present invention relates to a nonvolatile semiconductor memory device in which shallow trench isolation is formed in a self-aligned manner with a polycrystal silicon layer for a floating gate electrode and which is capable of preventing occurrence of any kink characteristic in a transistor of a peripheral circuit portion.

A nonvolatile semiconductor memory device is known which incorporates stack-gate memory cells each having a control gate electrode and a floating gate electrode and peripheral circuits of the memory cells which are

integrated on one chip. In general, a semiconductor memory device of the foregoing type incorporates shallow trench isolation which is formed in a self-aligned manner with a polycrystal silicon layer of a floating gate electrode. The transistor of the peripheral circuit is again subjected to gate oxidation and formation of electrodes after the polycrystal silicon for a floating gate electrode has been removed.

When the polycrystal silicon for a floating gate electrode is removed, an end of the peripheral circuit region is exposed to outside. Thus, a gate electrode which is afterwards formed on the active region is sometimes undesirably formed on the side surface of the upper portion. If the gate electrode is formed on the side surface, a parasitic transistor is undesirably formed on the side surface of the active region. Thus, a so-called kink characteristic occurs such that a low threshold characteristic curve caused from the parasitic transistor is superimposed on the drain voltage-current characteristic of a MOSFET. If the parasitic transistor occurs, there arises a problem in that the electric current is increased during standby of the memory.

To prevent the kink characteristic, a multiplicity of bird's beaks must previously be formed between the active region and the polycrystal silicon layer. When electrons are drawn from the floating gate electrode

into the silicon substrate, the portion, the shape of which has been changed, encounters concentration of electric fields. It leads to a fact that erasing speed disperses among the cells. The dispersion of the erasing speed causes the width of the erasing Vth distribution to be increased. Hence it follows that a NOR-type flush memory encounters a problem of excessive erasing. If the memory cell is oxidized insufficiently such that bird's beaks are not formed, the gate electrode of the peripheral circuit falls in the STI. Thus, the kink characteristic occurs. Hence it follows that the sub-threshold leak is increased in the peripheral circuit. As a result, power consumption of the semiconductor memory device during standby is undesirably increased.

The foregoing problem will now be described with reference to FIGS. 24A-24D to 26A-26C.

A tunnel oxide film 102 is formed on a silicon substrate 101, and then a first polycrystal silicon 103 which serves as a lower portion of the floating gate electrode is deposited (see FIG. 24A). Then, a shallow trench (an STI region) 104 is formed to form a device isolation region (see FIG. 24B). At this time, the end of the floating gate electrode and the STI are formed in a self-aligned manner. Thus, the floating gate electrode does not fall in the STI trench and dispersion of the operation of the memory cells does

not easily take place. The inside portion of the STI region is embedded with an insulating film 105, and then a second polycrystal silicon layer 106 serving as the upper portion of the floating gate electrode is deposited. Then, isolation into cells is performed (FIG. 24C).

Then, the floating gate electrode and an insulating film 107 between control gate electrodes are formed, the insulating film 107 being a film which will be formed later. Usually, a three-layer structure film is formed which consists of an oxide film/nitride film/oxide film (see FIG. 24D). The following drawings show a process for forming the peripheral circuit.

The insulating film 107, the floating gate electrodes 103 and 106 and the tunnel oxide film 102 in the peripheral circuit portion are removed. In a wet etching process for removing the tunnel oxide film, the embedded insulating film 105 at the end of the STI is sometimes moved in a rearward direction. Thus, a recess is sometimes undesirably formed. In the foregoing case, the gate electrode 108 in the peripheral circuit reaches the side surface of the active region, as shown in FIGS. 25 and 26. Simultaneously, the gate electrode overlaps the edge of the active region in which concentration of electric fields occurs, causing a parasitic transistor to be formed. The parasitic transistor has a low threshold

characteristic which is superimposed on the drain voltage-current characteristic of the main transistor. Thus, the kink characteristic occurs.

As a method of preventing the foregoing problem, a method may be employed with which oxidation is sufficiently performed prior to formation of an embedded insulating film 205 in the STI. Thus, the bird's beaks 209 are, as shown in FIG. 27A, previously formed in the interface between the first polycrystal silicon and the silicon substrate. As a result, rearward movement of the insulating film in the end portion of the STI can be prevented as shown in FIG. 27B even after the polycrystal silicon and the tunnel oxide film have been removed. A polycrystal silicon layer 206 is a second polycrystal silicon layer forming an upper layer portion of the floating gate electrode. Reference numeral 207 denotes an insulating film, and reference numeral 208 denotes a polycrystal silicon layer.

If oxidation is sufficiently performed as described above, a fact has been detected that a critical problem arises. That is, as shown in FIGS. 27C and 28, when the bird's beaks are greatly introduced in between the floating gate electrode and the silicon substrate in the memory cell region, the shape is dispersed because the planar orientation of the polycrystal silicon varies. What is worse, projecting portions are formed owing to the oxidation,

causing electric fields to be concentrated to the projecting portions. If the shape is dispersed as described above, the drawing speed in, for example, an operation for drawing electrons from the floating gate electrode is undesirably varied. Thus, there arises a problem in that the erasing Vth distribution is widened. The wide erasing distribution causes the NOR-type flush memory to encounter a defective operation, such as excessive erasing.

As described above, a portion of the conventional STI nonvolatile semiconductor memory device has a structure that great bird's beaks are formed in the interface between the polycrystal silicon and the silicon substrate to prevent the kink characteristic of the transistor in the peripheral circuit. However, the bird's beak is sometimes introduced between the floating gate electrode in the memory cell portion and the silicon substrate. As a result, the drawing speed in the operation for drawing electrons from the floating gate electrode varies. Therefore, there arises a problem in that the erasing Vth distribution is widened.

BRIEF SUMMARY OF THE INVENTION

In view of the foregoing, an object of the present invention is to provide a nonvolatile semiconductor memory device which is capable of preventing dispersion of the characteristics of memory cell portion thereof

and occurrence of a kink characteristic in the peripheral circuit portion and which is free from enlargement of the power consumption during standby and a manufacturing method therefor.

To achieve the above object, according to an aspect of the present invention, there is provided a nonvolatile semiconductor memory device comprising a semiconductor substrate; a memory cell portion on the semiconductor substrate in which a plurality of memory cells each having a charge storage layer are formed; a peripheral circuit portion on the semiconductor substrate in which a circuit for controlling the memory cells is formed; a plurality of active regions formed in each of the memory cell portion and the peripheral circuit portion and isolated from one another by a plurality of trenches; insulating films with which the trenches are filled; bird's beak-shape oxide films formed between the active regions and the charge storage layers of the memory cell portion; and bird's beak-shape oxide films formed between the active regions and gate electrodes of the peripheral circuit portion, the bird's beak-shape oxide films being thicker than the bird's beak-shape oxide films formed between the active regions and the charge storage layers of the memory cell portion.

According to another aspect of the present invention, there is provided a nonvolatile semiconductor

memory device comprising a memory cell array portion of a semiconductor substrate in which a plurality of memory cell transistors are formed in active regions of the semiconductor substrate and the active regions of the memory cell transistors oppose gate electrodes thereof and are insulated and isolated by an embedded device isolating regions; and a peripheral transistor portion of the semiconductor substrate in which a plurality of peripheral transistors are formed in active regions of the semiconductor substrate and active regions of the peripheral transistors oppose gate electrodes thereof are insulated and isolated by an embedded device isolating regions, wherein the curvature of device isolating ends of the active region of the peripheral transistor is larger than the curvature of the device isolating ends of the active region of the memory cell transistor.

According to a further aspect of the present invention, there is provided a method of manufacturing a nonvolatile semiconductor memory device having constituted by a shallow trench isolation and including a memory cell portion having a charge storage layer and a peripheral circuit portion of the memory cell portion, the method of manufacturing a nonvolatile semiconductor memory device comprising the steps of forming a polycrystalline silicon layer on a silicon substrate through an insulating film; providing

a plurality of shallow trench isolation portions each having a bottom and formed to surround an active region for the silicon substrate by etching, in a self-aligned manner, the polysilicon layer, the insulating film and the silicon substrate in order to form an active region; rounding edges at the device isolating side of opposite surfaces of the active region and the polysilicon layer by oxidation; coating only the memory cell portion with a film having oxidation resistance; and performing further-oxidation, after only the memory cell portion has been coated with a film having oxidation resistance, to provide a bird's beak-shape oxide film, the thickness of which is larger than the thickness of a bird's beak-shape oxide film in the memory cell portion, between ends of the opposite surfaces of the silicon substrate and the polysilicon layer.

According to a further aspect of the present invention, there is provided a method of manufacturing a nonvolatile semiconductor memory device having an active region constituted by a shallow trench isolation and including a memory cell portion having a charge storage layer and a peripheral circuit portion of the memory cell portion, the method of manufacturing a nonvolatile semiconductor memory device comprising the steps of forming a polycrystalline silicon layer on a silicon substrate through an insulating film; providing

a plurality of shallow trench isolation portions each having a bottom and formed to surround an active region for the silicon substrate by etching, in a self-aligned manner, the polysilicon layer, the insulating film and the silicon substrate in order to form an active region; rounding edges of opposite surfaces of the active region and the polysilicon layer by oxidation; coating only the memory cell portion with a film having oxidation resistance; selectively removing the oxidation resisting films so that the oxidation resisting films are left only on side walls of the charge storage layers and only on side walls of the trenches in the memory cell portion; and performing further-oxidation, after the oxidation resisting films has been selectively removed, to provide a bird's beak-shape oxide film, the thickness of which is larger than the thickness of a bird's beak-shape oxide film in the memory cell portion, between ends of the opposite surfaces of the silicon substrate and the polysilicon layer.

According to a further aspect of the present invention, there is provided a method of manufacturing a nonvolatile semiconductor memory device having an active region constituted by a shallow trench isolation and including a memory cell portion having a charge storage layer and a peripheral circuit portion of the memory cell portion, the method of manufacturing

a semiconductor memory device comprising the steps of forming a polysilicon layer on a silicon substrate through an insulating film; forming a first shallow trench isolation portion by, in a self-aligned manner, etching the polysilicon layer, the insulating film and the silicon substrate in only the peripheral circuit portion; forming a bird's beak-shape oxide film by oxidizing edges of opposite surfaces of the active region and the first polysilicon layer in the peripheral circuit portion; forming a second shallow trench isolation portion by, in a self-aligned manner, etching the polysilicon layer, the insulating film and the silicon substrate in the memory cell portion; and forming a bird's beak-shape oxide film, the thickness of which is smaller than the thickness of the bird's beak-shape oxide film formed in the peripheral circuit portion, by oxidizing ends of opposite surfaces of the active region and the polysilicon layer in the memory cell portion after the second shallow trench isolation portion has been formed.

According to a further aspect of the present invention, there is provided a method of manufacturing a nonvolatile semiconductor memory device having an active region constituted by a shallow trench isolation and including a memory cell portion having a charge storage layer and a peripheral circuit portion of the memory cell portion, the method of manufacturing

a nonvolatile semiconductor memory device comprising the steps of forming an oxidation resisting film on a silicon substrate through an insulating film; selectively removing the oxidation resisting film and the insulating film in the memory cell portion; forming a tunnel oxide film in the memory cell portion and nitrifying the tunnel oxide film to form the tunnel film into an oxi-nitride film; forming a polysilicon layer on the tunnel oxi-nitride film in the memory cell portion and the oxidation resisting film in the peripheral circuit portion; providing a shallow trench isolation portion for the memory cell portion and the peripheral circuit portion by, in a self-aligned manner, etching the polysilicon and the silicon substrate; and providing a bird's beak-shape oxide film, the thickness of which is larger than the thickness of the memory cell portion, for the peripheral circuit portion by providing a bird's beak-shape oxide film for ends of opposite surfaces of the active region and the polysilicon layer by performing oxidation after the shallow trench isolation has been formed.

According to a further aspect of the present invention, there is provided a method of manufacturing a nonvolatile semiconductor memory device having an active region constituted by a shallow trench isolation and including a memory cell portion having a charge

storage layer and a peripheral circuit portion of the memory cell portion, the method of manufacturing a nonvolatile semiconductor memory device comprising the steps of forming a polysilicon layer on a silicon substrate through an insulating film; forming a shallow trench isolation portion to form an active region by, in a self-aligned manner, etching the polysilicon layer and the silicon substrate; rounding ends of opposite surfaces of the active region and the polysilicon by oxidation; coating only the memory cell portion with a silicon film; performing further-oxidation after coating with the silicon film has been performed to provide a bird's beak-shape oxide film, the thickness of which is larger than the thickness of the memory cell portion, for a space between ends of opposite surfaces of the silicon substrate and the polysilicon layer in the peripheral circuit portion; and forming the silicon film covering the memory cell portion into an oxide film.

According to a further aspect of the present invention, there is provided a method of manufacturing a nonvolatile semiconductor memory device having an active region constituted by a shallow trench isolation and including a memory cell portion having a charge storage layer and a peripheral circuit portion of the memory cell portion, the method of manufacturing a nonvolatile semiconductor memory device comprising

the steps of forming a polysilicon layer serving as an insulating film and a charge storage layer for a silicon substrate; forming a shallow trench isolation portions by etching the polysilicon layer and the silicon substrate in a self-aligned manner; and forming a silicon oxi-nitride film on the inner walls of the trenches and the side walls of the polysilicon layer.

According to a further aspect of the present invention, there is provided a method of manufacturing a semiconductor apparatus such that a portion of gate insulating film of MOS transistor is formed before formation of a device isolation and a remaining portion of the gate insulating film is formed after formation of the device isolation, the method of manufacturing a semiconductor apparatus comprising the step of forming an MOS transistor in such a manner that the curvature of ends of an active region of the MOS transistor having a gate insulating film which is formed after formation of the device isolation is larger than the curvature of the end of an active region of the MOS transistor having a gate insulating film which is formed before formation of the device isolation.

Additional objects and advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention may be realized and

obtained by means of the instrumentalities and combinations particularly pointed out hereinafter.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate presently preferred embodiments of the invention, and together with the general description given above and the detailed description of the preferred embodiments given below, serve to explain the principles of the invention.

FIGS. 1A-1D are cross sectional views sequentially showing a method of manufacturing a semiconductor memory device according to a first embodiment of the present invention;

FIGS. 2A-2C are cross sectional views showing processes following the process shown in FIG. 1D;

FIGS. 3A-3C are cross sectional views showing processes following the process shown in FIG. 2C;

FIGS. 4A-4D are cross sectional views showing processes following the process shown in FIG. 3C;

FIG. 5 is a cross sectional view showing a process of a modification of the manufacturing method shown in FIGS. 1A-4D;

FIGS. 6A-6O are cross sectional views sequentially showing a method of manufacturing a semiconductor memory device according to a second embodiment of the present invention;

FIGS. 7A-7C are cross sectional views sequentially showing a method of manufacturing a semiconductor memory device according to a third embodiment of the present invention;

FIGS. 8A-8B are cross sectional views showing processes following the process shown in FIG. 7C;

FIGS. 9A-9D are cross sectional views sequentially showing a method of manufacturing a semiconductor memory device according to a fourth embodiment of the present invention;

FIGS. 10A-10C are cross sectional views showing processes following the process shown in FIG. 9D;

FIGS. 11A-11D are cross sectional views sequentially showing a method of manufacturing a semiconductor memory device according to a fifth embodiment of the present invention;

FIGS. 12A-12C are cross sectional views showing processes following the process shown in FIG. 11D;

FIGS. 13A-13C are cross sectional views showing processes following the process shown in FIG. 12C;

FIGS. 14A-14D are cross sectional views showing processes following the process shown in FIG. 13C;

FIGS. 15A-15D are cross sectional views sequentially showing a method of manufacturing a semiconductor memory device according to a sixth embodiment of the present invention;

FIGS. 16A-16C are cross sectional views showing

processes following the process shown in FIG. 15D;

FIGS. 17A-17D are cross sectional views showing processes following the process shown in FIG. 16C;

FIGS. 18A-18D are cross sectional views showing a portion of a process for manufacturing a NOR-type flush EEPROM according to a seventh embodiment of the present invention;

FIGS. 19A-19D are cross sectional views showing a portion of a process following the process shown in FIG. 18D;

FIGS. 20A and 20B are cross sectional views showing an example of the shape marked with a circle shown in FIG. 19C and an example of the shape of the foregoing portion realized after the device has been manufactured, respectively;

FIGS. 21A-21C are cross sectional views showing a portion of a process for manufacturing a NOR-type flush EEPROM according to an eighth embodiment of the present invention;

FIGS. 22A-22D are cross sectional views showing a portion of a process following the process shown in FIG. 21C;

FIG. 23 is an enlarged cross sectional view showing a portion marked with a circle shown in FIG. 22C;

FIGS. 24A-24D are cross sectional views sequentially showing a method of manufacturing

a conventional semiconductor memory device;

FIG. 25 is a cross sectional view showing a parasitic transistor occurring in the conventional semiconductor memory device;

FIG. 26 is an enlarged cross sectional view of a portion of the conventional semiconductor memory device shown in FIG. 25;

FIGS. 27A-27C are cross sectional views showing a method of providing bird's beaks for the conventional semiconductor memory device and problems experienced with the conventional method; and

FIG. 28 is an enlarged cross sectional view of a portion of the conventional semiconductor memory device shown in FIG. 27C.

DETAILED DESCRIPTION OF THE INVENTION

Embodiments of the present invention will now be described with reference to the drawings.

First Embodiment

FIGS. 1A-1D to 4A-4D are diagrams sequentially showing a method of manufacturing a semiconductor memory device according to a first embodiment of the present invention, and cross sectional views showing a peripheral circuit portion.

Initially, a tunnel oxide film 302 of memory cells is formed on the overall surface of a silicon substrate 301 to have a thickness of, for example, 10 nm. A first polycrystal silicon layer 303 serving as a

lower portion of a floating gate electrode as a charge storage layer is formed on the tunnel oxide film 302 to have a thickness of 70 nm (see FIG. 1A). Then, a silicon nitride film 304 is usually deposited on the first polycrystal silicon layer 303 to have a thickness of, for example, 200 nm. Then, a photolithography process is performed to form a resist pattern having opened portions in which shallow trench isolation portions are formed. In accordance with the resist pattern, the silicon nitride film 304 is processed (see FIG. 1B).

Then, the silicon nitride film 304 is used as a mask to sequentially and vertically etch the first polycrystal silicon layer 303 for a floating gate electrode, the tunnel oxide film 302 and the silicon substrate 301 by a RIE method. Shallow trenches 305 formed in the silicon substrate 301 are shallow trench isolation (STI).

Then, oxidation, for example, thermal oxidation is performed to have a thickness of 10 nm such that the amount of oxidation is minimized to prevent formation of bird's beaks in the interface between the first polycrystal silicon layer 303 serving as the floating gate electrode and the silicon substrate 301. Thus, a thermally-oxidized film 306 is formed (see FIG. 1C).

Then, an oxide film 307 is deposited by a CVD method to have a small thickness. Then, an oxidation

resisting film, specifically, a silicon nitride film 308 is deposited on the oxide film 307 to have a thickness of 6 nm (see FIG. 1D).

A resist pattern 309 opened in only the peripheral circuit portion is formed on the substrate by a photolithography process (see FIG. 2A). The resist pattern 309 is used as a mask to remove the oxidation resisting film 308 in the peripheral circuit portion (see FIG. 2B). When the oxidation resisting film 308 is the silicon nitride film, it can be removed by a method, for example, CDE (Chemical Dry Etching). The CVD oxide film 307 formed below the oxidation resisting film reduces the degree of damage sustained in the silicon substrate when an embedded film is deposited in the device isolating trench.

Then, oxidation is performed for foregoing bird's beaks into the end portions of opposite surfaces of the active region of the silicon substrate 301 and the first polycrystal silicon layer 303 in the peripheral circuit portion (see FIG. 2C). The active region includes a channel region and source/drain regions of an MOS transistor. Bird's beaks 310 formed by the oxidation reduce the degree of falling of a gate electrode when a following process for forming the peripheral circuit is performed. Therefore, the oxidation is performed in a sufficiently large quantity such that an oxide film having a thickness of, for

example, 30 nm is formed on the silicon substrate 301.

At this time, the memory cell portion is not oxidized because the memory cell portion is covered with the oxidation resisting film 308. Accordingly, bird's beaks are not formed into the end portions of opposite surfaces of the active region (the silicon substrate 301) and the first polycrystal silicon layer 303 in the memory cell portion. If necessary, the oxidation resisting film 308 may be removed at a later step, as shown in FIG. 5. If a silicon nitride film is present in the vicinity of the memory cell, there is apprehension that the tunnel oxide film sustains damage owing to hydrogen diffused from the silicon nitride film. Therefore, the silicon nitride film may be removed if necessary. In this embodiment, the silicon nitride film is not removed. When the silicon nitride film is removed, etching or CDE using hot phosphoric acid is performed after the process shown in FIG. 1D.

Then, for example, a plasma oxide film 311 is deposited to embed the device isolating trench (see FIG. 3A). When a structure having a high aspect ratio is manufactured, a high-density plasma (HDP) CVD method is sometimes employed to deposit the plasma oxide film 311. Then, the plasma oxide film 311 is smoothed by, for example, a CMP (Chemical Mechanical Polishing) method (see FIG. 3B).

Then, the silicon nitride film 304 formed on the

first polycrystal silicon layer 303 for the floating gate electrode is removed by performing wet etching. In some cases, the insulating film 311 is somewhat etched before the nitride film is removed in order to adjust the height of the insulating film 311 embedded in the device isolating trench. Then, a second polycrystal silicon layer 312 for the floating gate electrode is formed. Then, lithography and etching of the region 313 for isolating the floating gate electrode are performed in the STI region to perform a process for isolating the floating gate electrode for each cell (see FIG. 3C).

Then, a laminated insulating film 314 in the form of, for example, oxide film/nitride film/oxide film (ONO) serving as an insulating film between the floating gate electrode and the control gate electrode is formed on the floating gate electrode (FIG. 4A). Then, drawings show only the peripheral circuit portion.

Then, the memory cell region is coated with a resist by photolithography. Then, the ONO film 314, the first and second polycrystal silicon layers 303 and 312 for the floating gate electrode in the peripheral circuit region are removed by dry etching. The tunnel oxide film 302 is removed by wet etching (see FIG. 4B). Since the gate bird's beaks have sufficiently been formed, upper ends of the active region are protected

when the wet etching is performed. Therefore, falling of the oxide film at the upper ends can be prevented.

Then, a gate oxide film 315 having a required thickness of 15 nm is formed on the substrate surface of the peripheral circuit (see FIG. 4C). Then, a polycrystal silicon layer 316 is formed on the gate oxide film 315 (see FIG. 4D). The polycrystal silicon layer 316 is patterned so that a gate electrode for the peripheral circuit and the control gate electrode for the memory cell portion are formed.

Then, gates of the peripheral transistors and the memory cell transistors are formed by a method (not shown). Then, a usual process is performed so that a diffusion layer is provided for each the memory cell portion and the peripheral circuit portion. Then, a wiring process is performed. Thus, a memory cell array is manufactured.

After the foregoing processes have been performed, a semiconductor memory device having bird's beaks greatly introduced into only the peripheral circuit portion is realized, while substantially not having bird's beaks introduced into the memory cell portion. That is, the curvature of ends of the active region of the peripheral circuit portion is substantially larger than the curvature of ends of the active region of the memory cell portion.

Second Embodiment

In the first embodiment, the overall surface of the memory cell region is covered with the silicon nitride film. When the overall surface is covered with the silicon nitride film and heat treatment is performed, the tunnel oxide film 302 in the memory cell sometimes deteriorates. To minimize the foregoing phenomenon, the oxidation resisting film in the form of side walls may be formed on the side surfaces of the floating gate electrode of the memory cell.

A second embodiment of the present invention providing the foregoing method will be described with reference to FIGS. 6A-6O. FIGS. 6A-6O are cross sectional views sequentially showing a method of manufacturing a semiconductor memory device according to the first embodiment of the present invention.

Initially, processes shown in FIGS. 6A to 6D similar to the processes shown in FIGS. 1A to 1D of the first embodiment are performed. Specifically, a tunnel oxide film 302 of memory cells is formed on the overall surface of a silicon substrate 301 to have a thickness of, for example, 10 nm. A first polycrystal silicon layer 303 serving as a lower portion of a floating gate electrode is formed on the tunnel oxide film 302 to have a thickness of 70 nm (see FIG. 6A). Then, a silicon nitride film 304 is usually deposited on the first polycrystal silicon layer 303 to have a thickness of, for example, 200 nm. Then, a photolithography

process is performed to form a resist pattern having opened portions in which shallow trench isolation portions are formed. In accordance with the resist pattern, the silicon nitride film 304 is processed (see FIG. 6B).

Then, the silicon nitride film 304 is used as a mask to sequentially and vertically etch the first polycrystal silicon layer 303 for a floating gate electrode, the tunnel oxide film 302 and the silicon substrate 301 by a RIE method. Shallow trenches 305 formed in the silicon substrate 301 are shallow trench isolation (STI) for device isolation.

Then, oxidation, for example, thermal oxidation is performed to have a thickness of 10 nm such that the amount of oxidation is minimized to prevent formation of bird's beaks in the interface between the first polycrystal silicon layer 303 serving as the floating gate electrode and the silicon substrate 301. Thus, a thermally-oxidized film 306 is formed (see FIG. 6C).

Then, an oxide film 307 is deposited by a CVD method to have a small thickness. Then, an oxidation resisting film, specifically, a silicon nitride film 308 is deposited on the oxide film 307 to have a thickness of 6 nm (see FIG. 6D).

After the oxidation resisting film 308 has been deposited in the process shown in FIG. 6D, then etching back of the overall surface is performed by the RIE

method so that the oxidation resisting film 308 is left only on the side wall of the polycrystal silicon layer 303 and only on the side wall of the device isolating trench. Thus, a structure shown in FIG. 6E is obtained.

Thereafter, processes similar to those shown in FIGS. 2A-2C and following drawings 3A-4D of the first embodiment are performed. As a result, a structure in which the oxidation resisting film is left on only the side walls of the floating gate electrode and only on the side wall of the shallow trench can be manufactured. Specifically, a resist pattern 309 opened in only the peripheral circuit portion is formed on the substrate by a photolithography process (see FIG. 6F). The resist pattern 309 is used as a mask to remove the oxidation resisting film 308 in the peripheral circuit portion (see FIG. 6G). When the oxidation resisting film 308 is the silicon nitride film, it can be removed by a method, for example, CDE (Chemical Dry Etching). The CVD oxide film 307 formed below the oxidation resisting film reduces the degree of damage sustained in the silicon substrate when an embedded film is deposited in the device isolating trench.

Then, oxidation is performed for foregoing bird's beaks into the end portions of opposite surfaces of the active region (the silicon substrate 301) and the first polycrystal silicon layer 303 in the peripheral circuit

portion (see FIG. 6H). Bird's beaks 310 formed by the oxidation reduce the degree of falling of a gate electrode when a following process for forming the peripheral circuit is performed. Therefore, the oxidation is performed in a sufficiently large quantity such that an oxide film having a thickness of, for example, 30 nm is formed on the silicon substrate 301.

At this time, the memory cell portion is not oxidized because the side walls of the floating gate electrode and the side wall of the shallow trench of the memory cell portion is covered with the oxidation resisting film 308. Accordingly, bird's beaks are not formed into the end portions of opposite surfaces of the active region (the silicon substrate 301) and the first polycrystal silicon layer 303 in the memory cell portion. If necessary, the oxidation resisting film 308 may be removed at a later step, as shown in FIG. 5. If a silicon nitride film is present in the vicinity of the memory cell, there is apprehension that the tunnel oxide film sustains damage owing to hydrogen diffused from the silicon nitride film. Therefore, the silicon nitride film may be removed if necessary. In this embodiment, the silicon nitride film is not removed. When the silicon nitride film is removed, etching or CDE using hot phosphoric acid is performed after the process shown in FIG. 6H.

Then, for example, a plasma oxide film 311 is

deposited to embed the device isolating trench (see FIG. 6I). When a structure having a high aspect ratio is manufactured, a high-density plasma (HDP) CVD method is sometimes employed to deposit the plasma oxide film 311. Then, the plasma oxide film 311 is smoothed by, for example, a CMP (Chemical Mechanical Polishing) method (see FIG. 6J).

Then, the silicon nitride film 304 formed on the first polycrystal silicon layer 303 for the floating gate electrode is removed by performing wet etching. In some cases, the insulating film 311 is somewhat etched before the nitride film is removed in order to adjust the height of the insulating film 311 embedded in the device isolating trench. Then, a second polycrystal silicon layer 312 for the floating gate electrode is formed. Then, lithography and etching of the region 313 for isolating the floating gate electrode are performed in the STI region to perform a process for isolating the floating gate electrode for each cell (see FIG. 6K).

Then, a laminated insulating film 314 in the form of, for example, oxide film/nitride film/oxide film (ONO) serving as an insulating film between the floating gate electrode and the control gate electrode is formed on the floating gate electrode (see FIG. 6L). Then, drawings show only the peripheral circuit portion.

Then, the memory cell region is coated with a resist by photolithography. Then, the ONO film 314, the first and second polycrystal silicon layers 303 and 312 for the floating gate electrode in the peripheral circuit region are removed by dry etching. The tunnel oxide film 302 is removed by wet etching (see FIG. 6M). Since the gate bird's beaks have sufficiently been formed, upper ends of the active region are protected when the wet etching is performed. Therefore, falling of the oxide film at the upper ends can be prevented.

Then, a gate oxide film 315 having a required thickness of 15 nm is formed on the substrate surface of the peripheral circuit (see FIG. 6N). Then, a polycrystal silicon layer 316 is formed on the gate oxide film 315 (see FIG. 6O). The polycrystal silicon layer 316 is patterned so that a gate electrode for the peripheral circuit and the control gate electrode for the memory cell portion are formed.

Then, gates of the peripheral transistors and the memory cell transistors are formed by a method (not shown). Then, a usual process is performed so that a diffusion layer is provided for each the memory cell portion and the peripheral circuit portion. Then, a wiring process is performed. Thus, a memory cell array is manufactured.

As in the first embodiment of the present invention, after the foregoing processes have been

performed, a semiconductor memory device having bird's beaks greatly introduced into only the peripheral circuit portion is realized, while substantially not having bird's beaks introduced into the memory cell portion. That is, the curvature of ends of the active region of the peripheral circuit portion is substantially larger than the curvature of ends of the active region of the memory cell portion.

Third Embodiment

FIGS. 7A-7C, 8A and 8B are cross sectional views sequentially showing a method of manufacturing a semiconductor memory device according to a third embodiment of the present invention.

A tunnel oxide film 502 of a memory cell is formed on the overall surface of a silicon substrate 501 to have a thickness of, for example, 10 nm. Then, a first polycrystal silicon layer 503 serving as a portion of a floating gate electrode is formed on the tunnel oxide film 502 to have a thickness of 70 nm (see FIG. 7A). Then, a silicon nitride film 504 is deposited on the first polycrystal silicon layer 503 to have a thickness of 200 nm (see FIG. 7B). Then, a photolithography process is performed so that a resist pattern (not shown) having opened portions in which the STI is formed is formed in the peripheral circuit portion so that the silicon nitride film 504 is processed. Then, the nitride film 304 is used as a mask to sequentially

and vertically etch the first polycrystal silicon layer 503 for the floating gate electrode, the tunnel oxide film 502 and the silicon substrate 501 by the RIE method so that an STI 505 is formed.

Then, oxidation is performed to have a thickness of, for example, 30 nm in order to form a sufficient bird's beak oxide film 506 in the interface between the polycrystal silicon layer 503 in the peripheral circuit portion and the silicon substrate 501 (see FIG. 7C). At this time, the surface of the memory cell portion covered with the silicon nitride film 504 is not oxidized.

Then, an STI 507 in the memory cell portion is formed (see FIG. 8A). Then, oxidation is performed to have a thickness of, for example, 6 nm to 10 nm required for the memory cell so that an oxide film 508 is formed (see FIG. 8B). Then, the process similar to that according to the first embodiment and shown in FIGS. 3A-3C are performed to form the embedded insulating film in the device isolating trench.

After the foregoing processes have been performed, a semiconductor memory device having bird's beaks greatly introduced into only the peripheral circuit portion is realized, while substantially not having bird's beaks introduced into the memory cell portion. That is, the curvature of ends of the active region of the peripheral circuit portion is substantially larger

than the curvature of ends of the active region of the memory cell portion.

Fourth Embodiment

FIGS. 9A-9D and 10A-10C are cross sectional views sequentially showing a method of manufacturing a semiconductor memory device according to a fourth embodiment of the present invention.

Initially, a first thick oxide film, for example, an oxide film 602 having the thickness of 20 nm is formed on a silicon substrate 601 (see FIG. 9A). Then, an oxidation resisting film, for example, a silicon nitride film 603 is deposited on the oxide film 602 to have a thickness of 8 nm (see FIG. 9B).

Then, lithography is performed to left a resist 604 in the peripheral circuit portion and to remove the silicon nitride film 603 in the memory cell portion (see FIG. 9C). Then, the resist is removed, and then the silicon oxide film having the thickness of 20 nm in the memory cell portion is removed by etching.

Then, a tunnel oxide film 605 is formed in the memory cell portion to have a thickness of, for example, 9 nm. Since the oxidation resisting film (the silicon nitride film) 603 is present in the peripheral circuit portion, no change occurs. Then, nitrogen is introduced in between the tunnel oxide film 605 and the silicon substrate 601 (see FIG. 9D). The nitrifying process prevents introduction of the bird's beak in the

following process. Since the tunnel oxide film is formed into oxynitride, the reliability of the cell can be improved. Since the peripheral circuit portion has been covered with the nitride film 603, the interface between the first oxide film 602 and the silicon substrate 601 is not nitrified. In general, nitrifying can be realized by performing heat treatment in a gas, such as ammonia, N_2O or NO.

Then, a first polycrystal silicon layer 606 serving as the lower portion of the floating gate electrode is formed on the oxidation resisting film 603 to have a thickness of 70 nm (see FIG. 10A). Then, a silicon nitride film 607 is, in general, deposited on the first polycrystal silicon layer 606 to have a thickness of, for example, 200 nm. Then, lithography is performed to form a resist pattern opened to correspond to the portions in which the STI is formed. Then, the silicon nitride film 607 is processed.

Then, the nitride film 607 is used as a mask to sequentially and vertically etch the first polycrystal silicon layer 606 for the floating gate electrode, the silicon nitride film 603, the first oxide film 602 serving as the base layer and the silicon substrate 601 in the peripheral circuit portion by the RIE method. Also the polycrystal silicon layer 606, the tunnel oxide film 605 and the silicon substrate 601 in the memory cell portion are sequentially and vertically

etched by the RIE method. The shallow trenches formed in the silicon substrate are the shallow trench isolation (STI)(see FIG. 10B).

Then, oxidation is performed in order to introduce bird's beaks into the ends of the interface between the active region and the silicon nitride film 603 in the peripheral circuit portion (see FIG. 10C). The oxidation process causes the oxide films 609 and 610 to be formed. Bird's beaks 610 in the peripheral circuit portion can prevent falling of the gate electrode when the peripheral circuit is formed afterwards. Therefore, the oxidation process is performed in an efficient quantity. At this time, the bird's beak cannot easily be introduced into the memory cell portion because the tunnel oxide film has been nitrified.

Since the thick silicon oxide film 602 which is not nitrified is present on the active region in the peripheral circuit portion, a bird's beak 610 thicker than that of the bird's beak in the memory cell portion can be introduced into the interface between the silicon substrate 601 and the silicon oxide film 602. Note that the thick silicon oxide film 602 in the peripheral circuit portion and the silicon nitride film 603, 606, and 607 on the thick silicon oxide film 602 are completely removed before the gate oxide film in the peripheral circuit portion is formed (corresponding

to the process according to the first embodiment and shown in FIG. 4B).

After the foregoing processes have been performed, a semiconductor memory device having bird's beaks greatly introduced into only the peripheral circuit portion is realized, while substantially not having bird's beaks introduced into the memory cell portion. That is, the curvature of ends of the active region of the peripheral circuit portion is substantially larger than the curvature of ends of the active region of the memory cell portion.

Fifth Embodiment

FIGS. 11A-11D to FIGS. 14A-14D are cross sectional views sequentially showing a method of manufacturing a semiconductor memory device according to a fifth embodiment of the present invention.

Initially, a tunnel oxide film 702 for the memory cell is formed on the overall surface of the silicon substrate 701 to have a thickness of, for example, 10 nm. Then, a first polycrystal silicon layer 703 serving as the lower portion of the floating gate electrode is formed on the tunnel oxide film 702 to have a thickness of 70 nm (see FIG. 11A).

Then, a silicon nitride film 704 is usually deposited on the first polycrystal silicon layer 703 to have a thickness of, for example, 200 nm. Then, photolithography is performed to form a pattern opened

to correspond to the portions in which the STI is formed. Then, the silicon nitride film is processed. Then, the nitride film is used as a mask to sequentially process the first polycrystal silicon layer for the floating gate electrode, the tunnel oxide film and the silicon substrate by the RIE method. The shallow trenches formed in the silicon substrate are shallow trench isolation (STI)(see FIG. 11B).

Then, oxidation is performed in a minimum quantity in such a manner that the bird's beak is not greatly introduced into the interface between the first polycrystal silicon serving as the floating gate electrode and the silicon substrate. For example, thermal oxidation is performed to have a thickness of 10 nm. Thus, a thermally oxidized film 706 is formed (see FIG. 11C).

Then, an oxide film 707 is deposited on the thermally oxidized film 706 by a CVD method. Specifically, an amorphous silicon film 708 is deposited to have a thickness of 10 nm by, for example, a low-pressure CVD (LPCVD) method (see FIG. 11D).

Then, photolithography is performed to form a resist pattern 709 opened in only the peripheral portion (see FIG. 12A). The resist material is used as a mask to remove the silicon film 708 in the peripheral circuit portion (see FIG. 12B). If the silicon film 708 is the amorphous silicon film, the CDE method or

the like is employed to remove the amorphous silicon film. Note that the CVD oxide film 707 formed below the silicon film reduces the degree of damage introduced into the silicon substrate when the embedded insulating film is afterwards deposited in the device isolating trench.

Then, oxidation is performed in order to introduce the bird's beak into the edges of the STI in the peripheral circuit portion (see FIG. 12C). The bird's beak 710 formed by the foregoing oxidation process can reduce the degree of falling of the gate electrode when the peripheral circuit portion is formed afterwards. Therefore, the oxidation process is performed in a sufficiently large quantity. For example, an oxide film having a thickness of

30 nm is formed on the silicon substrate.

The memory cell portion is covered with the amorphous silicon film 708 and completely oxidized when the bird's beak at the top end of the active region in the peripheral circuit portion is oxidized. Moreover, the amorphous silicon film 708 is formed into a silicon oxide film 711 having a thickness of 20 nm which is about two times.

In the memory cell portion, the amorphous silicon film 708 is completely formed into the silicon oxide film 711. Then, an oxidizer diffuses the silicon oxide film 711 to oxidize the silicon substrate 701 and the

first polycrystal silicon film 703 which is the lower portion of the floating gate electrode.

The oxidizer, which diffuses the silicon oxide film 711 and the silicon oxide film 706 formed by the CVD method, however reaches the silicon substrate 701 or the polycrystal silicon film 703. Therefore, the oxidizing rate of the silicon substrate 701 and the first polycrystal silicon film 703 which is the lower portion of the floating gate electrode is considerably lowered. Hence it follows that the bird's beak is not substantially introduced into the upper end portion of the active region of the memory cell portion in the foregoing process.

The amount of oxidation to introduce the bird's beak into the upper end portion of the active region in the peripheral circuit portion must be equivalent to the amount of oxidation required for the silicon film 708 deposited on the memory cell portion to completely be formed into the silicon oxide film 711. Moreover, introduction of the bird's beak into the upper end portion of the active region in the memory cell portion must substantially be prevented. In consideration of the foregoing facts, the thickness of the silicon oxide film 708 which is formed by deposition is determined.

To embed the inside portion of the STI afterwards, for example, a plasma oxide film 712 is deposited (see FIG. 13A). When the aspect ratio is high, a

high-density plasma (HDP) CVD is sometimes employed to perform the depositing process. Then, for example, CMP method is employed to smooth the plasma oxide film (see FIG. 13B).

Then, the silicon nitride film 704 on the first polycrystal silicon 703 for the floating gate electrode is removed by wet etching. In some cases, the insulating film 712 is somewhat etched before the nitride film 704 is removed to adjust the height of the insulating lithography 712 embedded in the device isolating trench.

Then, a second polycrystal silicon layer 713 for the floating gate electrode is formed. Then, lithography and etching of the floating gate isolating region 714 are performed in the STI region to perform a process for isolating the floating gate electrode for each cell (see FIG. 13C).

Then, a laminated insulating film 715 in the form, for example, oxide film/nitride film/oxide film (ONO) and serving as an insulating film between the floating gate electrode and the control gate electrode is formed on the floating gate electrode 713 (see FIG. 14A). Then, only the peripheral circuit portion is illustrated in the following drawings.

Then, the memory cell portion is covered with a resist by performing photolithography. Then, the ONO film 715 in the peripheral circuit portion and the

first and second polycrystal silicon 703, 715 for the floating gate electrode are removed by dry etching. The tunnel oxide film is removed by wet etching (see FIG. 14B). Since the bird's beak has sufficiently been formed when the wet etching process is performed, the upper end portion of the active region can be protected. Thus, falling of the oxide film at the upper end portion can be prevented.

Then, a gate oxide film 716 having a thickness required for the peripheral circuit portion, for example, 15 nm is formed (see FIG. 14C). Then, a polycrystal silicon layer 717 is formed on the gate oxide film 716 (see FIG. 14D). The polycrystal silicon layer 717 serves as a gate electrode for the peripheral circuit portion and the control gate electrode for the memory cell.

Then, gates for the peripheral transistors and the memory cell transistors are processed by a method (not shown). Then, a usual process is performed such that the diffusion layer is provided for the memory cell portion and the peripheral circuit portion. Then, a wiring process is performed. As a result, a memory cell array is manufactured.

After the foregoing processes have been performed, a semiconductor memory device having bird's beaks greatly introduced into only the peripheral circuit portion is realized, while substantially not having

bird's beaks introduced into the memory cell portion. That is, the curvature of ends of the active region of the peripheral circuit portion is substantially larger than the curvature of ends of the active region of the memory cell portion.

Sixth Embodiment

FIGS. 15A-15D to 17A-17D are cross sectional views sequentially showing a method of manufacturing a semiconductor memory device according to a sixth embodiment of the present invention. This embodiment is different from the first to fifth embodiments in that the large bird's beak is not formed in the upper end portion of the active region in the peripheral circuit portion. In this embodiment, the sidewalls of the STI in the peripheral circuit portion are covered with oxi-nitride films to prevent exposure of the side surfaces of the active region when the embedded insulating film in the device isolating trench is etched back. Thus, falling of the gate electrode in the peripheral circuit portion to the side surfaces of the active region can be prevented.

Referring to the drawings, a manufacturing process will now be described. FIGS. 15A-15D and 17A are diagrams which are applied to both of the memory cell portion and the peripheral circuit portion. FIGS. 17B to 17D are diagrams which are applied to the peripheral circuit portion.

Initially, a silicon oxide film 802 serving as a tunnel oxide film for the memory cell is formed on the overall surface of a silicon substrate 801 to have a thickness of, for example, 10 nm. Then, a first polycrystal silicon layer 803 serving as the lower portion of the floating gate electrode is formed on the silicon oxide film 802 to have a thickness of 70 nm (see FIG. 15A).

Then, a silicon nitride film 804 is usually deposited on the first polycrystal silicon layer 803 to have a thickness of, for example, 200 nm. Then, photolithography is performed to form a resist pattern opened to correspond to the portions in which the STI is formed. Then, the silicon nitride film is processed. Then, the nitride film is used as a mask to sequentially process the first polycrystal silicon for the floating gate electrode, the tunnel oxide film and the silicon substrate by the RIE method. The shallow trenches formed in the silicon substrate are the shallow trench isolation (STI)(see FIG. 15B).

Then, oxidation is performed in a minimum quantity, for example, a thermal oxidation process is performed in a quantity corresponding to a thickness of, for example, 10 nm in order to prevent great introduction of the bird's beak into the interface between the first polycrystal silicon serving as the floating gate electrode and the silicon substrate.

Thus, a thermally oxidized film 806 is formed (see FIG. 15C).

Then, a silicon oxide film 807 is deposited to have a thickness of 20 nm by the CVD method. Then, a process for changing the silicon oxide films 806 and 807 into the thermally oxidized film is performed (see FIG. 15D). Specifically, a process is performed for 60 minutes in an NH_3 atmosphere at, for example, 900℃. Then, a process is performed for 60 minutes in an O_2 atmosphere at 900℃. As a result of the foregoing processes, the interface region between the silicon oxide film 806 and silicon and the surface region of the silicon oxide film 807 are formed into oxi-nitride film containing nitrogen by several percents.

Then, for example, a plasma oxide film 812 is deposited to embed the inside portion of the STI (see FIG. 16A). When the aspect ratio is high, a high-density plasma (HDP) CVD is sometimes employed to perform the depositing process. Then, for example, the CMP method is employed to smooth the plasma oxide film (see FIG. 16B).

Then, the silicon nitride film 804 on the first polycrystal silicon 803 for the floating gate electrode is removed by wet etching. In some cases, the insulating film 812 is somewhat etched before the nitride film 804 is removed to adjust the height of the insulating film 812 embedded in the device isolating

trench. Then, a second polycrystal silicon layer 813 for the floating gate electrode is formed on the overall surface of the substrate. Then, lithography and etching of the floating gate insulating region 814 are performed in the STI region. Then, a process for isolating the floating gate electrode for each cell is performed (see FIG. 16C).

Then, a laminated insulating film 815 in the form of, for example, oxide film/nitride film/oxide film (ONO) and serving as an insulating film between the floating gate electrode and the control gate electrode is formed on the floating gate electrode 813 (see FIG. 17A). Hereinafter only the portion to be formed into the peripheral circuit is illustrated.

Then, the memory cell portion is covered with a resist (not shown). Then, the ONO film and the first and second polycrystal silicon layers 803 and 813 in the peripheral circuit portion are removed by dry etching. The tunnel oxide film 802 is removed by wet etching (see FIG. 17B). When the wet etching process is performed, the etching rate of the silicon sidewalls of the STI and the sidewalls of the first floating gate electrode 802 is lowered as compared with the etching rate of the tunnel oxide film 802 because the foregoing sidewalls are covered with the oxi-nitride films 806 and 807. Therefore, the sidewalls of the top end of the active region are not exposed.

Then, a gate oxide film 816 having a thickness of, for example, 15 nm which is required for the peripheral circuit portion is formed (see FIG. 17C). Then, a polycrystal silicon layer 817 is formed in the upper portion (see FIG. 17D). The polycrystal silicon layer serves as the gate electrode for the peripheral circuit portion and the control gate electrode for the memory cell.

In this embodiment, the silicon oxide film 806 is formed on the inner wall of the STI by performing an oxidizing process, followed by depositing the silicon oxide film 807. The necessity for forming the two silicon oxide films 806 and 807 may be eliminated. A deposited film or a single silicon oxide film formed by an oxidizing process may be employed.

Then, a process (not shown) of the gate electrodes of the peripheral transistors and the memory cell transistors is performed. Then, a usual process is performed such that a diffusion layer is provided for each of the memory cell and the peripheral circuit portion. Then, a wiring process is performed. Thus, a memory cell array is manufactured.

In this embodiment, the side surfaces of the upper end portion of the active region in the peripheral circuit portion after the gate electrode has been formed is covered with the oxi-nitride film formed on the inner wall of the STI. Thus, occurrence of the

kink characteristic of the peripheral transistor caused from reduction in the thickness of the oxide film can be prevented.

According to the first to fifth embodiments of the present invention, the bird's beak is not greatly formed between the active region of the memory cell and the silicon substrate. On the other hand, great bird's beaks can be provided for the peripheral circuit portion. Therefore, the degree of dispersion of the characteristics of the memory cells can be reduced. Since the bird's beaks are provided for the peripheral circuit, occurrence of the kink characteristic in the MOSFET can be prevented. Moreover, enlargement of the power consumption during standby can be prevented.

According to the six embodiments of the present invention, the inner wall of the STI is covered with the silicon oxi-nitride film. Therefore, reduction in the insulating film at the top end of the active region occurring when the tunnel oxide film is stripped in the peripheral circuit portion can be prevented. Thus, occurrence of the kink characteristic in the MOSFET can be prevented. As a result, enlargement of the power consumption during standby can be prevented.

Seventh Embodiment

FIGS. 18A-18D to 19A-19D are cross sectional views sequentially showing a method of manufacturing

a semiconductor device (a NOR-type flush EEPROM) according to a seventh embodiment of the present invention. The flush EEPROM has active regions insulated and isolated by embedded device isolation regions. The thickness of a gate oxide film of an MOS transistor in the memory cell array region and that in the peripheral transistor region are different from each other.

As shown in FIG. 18A, impurities are introduced in such a manner that the threshold value in the memory cell array region, i.e. a memory cell portion, of a semiconductor silicon substrate 901 and that in the peripheral transistor region, i.e. a peripheral circuit portion, become required values. Then, a gate oxide film 902 serving as a tunnel oxide film for the memory cell transistor is formed on the overall surface of the substrate. Then, a laminated film 904 is formed on the gate oxide film 902, the laminated film 904 being composed of a polysilicon film 903, a CVD nitride film and a CVD oxide film.

Then, a resist pattern (not shown) is formed on the substrate, the resist pattern being used to pattern the laminated film 904. Then, the resist pattern is removed.

Then, as shown in FIG. 18B, the patterned laminated film 904 is used as a mask to remove the polysilicon film 903, the gate oxide film 902 and the

silicon substrate 901 corresponding to the portion in which the device isolation region will be formed. Thus, shallow trenches are formed.

Then, the memory cell array region is covered with a resist (not shown), and then a wet etching (or isotropic etching or both of the foregoing processes) is performed. Thus, a portion (a portion on ends of the active region) of the gate oxide film 902 in the active region in the peripheral transistor region is removed as shown in FIG. 18C. Therefore, a shape which facilitates supply of an oxidizer into the ends of the active region is formed. On the other hand, any portion of the gate oxide film 902 in the active region in the memory cell transistor region is not removed.

Then, the resist is removed, and oxidation is performed in an atmosphere in which the temperature is, for example, 900℃ to 1000℃ and the concentration of oxygen is 10% in such a manner that the thickness of the oxidized portion in the surface of the trench is 20 nm or greater. Thus, an oxide film 913 is formed. At this time, the space between the end of the active region in the peripheral transistor region and the polysilicon film 903 on the ends is supplied with the oxidizer so that oxidation proceeds. Therefore, so-called bird's beaks are introduced and the ends of the active region are rounded, as shown in FIG. 18D. That is, the curvature of the device isolating ends of

the active region of the peripheral transistor becomes large. On the other hand, the curvature of the device isolating ends of the active region of the memory cell transistor does not become large, since any portion of the gate oxide film 902 in the active region in the memory cell transistor region is not removed. Accordingly, the curvature of device isolating ends of the active region of the peripheral transistor is larger than the curvature of the device isolating ends of the active region of the memory cell transistor.

Then, as shown in FIG. 19A, an embedded insulator, for example, an LP-TEOS film 905 is embedded in the trench. Then, a CMP method or an etch-back method is employed to smooth the overall surface so that the embedded insulator is backed to an intermediate portion of the laminated film 904. Then, wet etching is performed so that the laminated film 904 is removed.

Then, as shown in FIG. 19B, a polysilicon film 906 into which phosphorus has been introduced as the impurity is deposited on the overall surface of the substrate. Then, a resist pattern (not shown) is formed on the polysilicon film 906. The resist pattern is used to pattern the polysilicon film 906 so that a slit 907 for isolating the polysilicon film 906 in the memory cell array region on the device isolating region is formed. Thus, the polysilicon films 906 and 903 in the peripheral transistor region are removed.

Then, the resist pattern is stripped.

Then, an ONO insulating film 908 is formed on the overall surface of the substrate, and then the memory cell array region is covered with a resist (not shown). Then, the ONO insulating film 908 and the gate oxide film (the tunnel oxide film) 902 in the peripheral transistor region are removed. Then, the resist covering the memory cell array region is removed.

When the slit 907 is formed in the memory cell array region, the polysilicon films 906 and 903 in the peripheral transistor region may be left. Moreover, when the ONO insulating film 908 and the gate oxide film (the tunnel oxide film) 902 are removed, the polysilicon films 906 and 903 may be removed.

Then, a process similar to that of the conventional method is performed so that a gate oxide film 909 for the peripheral circuit transistor is formed, as shown in FIG. 19C. Then, a polysilicon film into which impurities have been introduced is deposited on the overall surface of the substrate.

In the memory cell array region, the polysilicon film, the ONO insulating film 908 and the polysilicon films 906 and 903 are patterned. Thus, as shown in FIG. 19D which is viewed from a direction perpendicular to FIG. 19C, a laminated gate structure incorporating two layer consisting of a control gate electrode 910 and a floating gate electrode 911 (the polysilicon

films 906 and 903) is formed. In the peripheral transistor region, the polysilicon film is patterned so that a gate electrode 912 is formed, as shown in FIG. 19D. Then, impurities serving as the source/drain of the transistor are selectively introduced into the surface layer of the substrate. Moreover, deposition of an interlayer insulating film, opening of a contact, wiring and deposition of a surface protective insulating film are performed. Thus, a flush EEPROM is manufactured.

FIG. 20A is an enlarged view showing the shape of an end corresponding to a portion marked with a circle drawn with a dashed line shown in FIG. 19C (that is, an end of an active region in a peripheral transistor region in which the gate oxide film has been formed after the formation of the device isolation insulating film). An example of an enlarged shape of the foregoing portion realized after the device has been manufactured is shown in FIG. 20B. Reference numeral 901 represents a semiconductor substrate, 905 represents a device isolation insulating film, 909 represents a gate oxide film and 912 represents a gate electrode.

As can be understood from FIGS. 20A and 20B, the gate oxide film 909 on the end of the active region includes the bird's beaks. Therefore, when the gate oxide films of the memory cell array region and the

gate oxide films of the peripheral circuit region are formed in different steps, reduction in the film at the end of the active region occurring in the stripping steps can be prevented as compared with the conventional structure having no bird's beak. As a result, concentration of electric fields at the end of the active region does not easily take place.

A shape of falling of the gate electrode 912 formed on the gate oxide film 909 at the end of the active region in the peripheral transistor region shown in FIGS. 20A and 20B is such that the amount of falling is smaller than that of the conventional structure. The measured difference d between the height of a flat portion in the active region and that of the lowest portion of the gate electrode upper than the flat portion was 4 nm or greater.

Eighth Embodiment

FIGS. 21A-21C and 22A-22D are cross sectional views sequentially showing a method of manufacturing a semiconductor device (a NOR-type flush EEPROM) according to an eighth embodiment of the present invention. The flush EEPROM incorporates active regions insulated and isolated by embedded device isolating regions. The thickness of the gate oxide film of the MOS transistor in the memory cell array region and that in the peripheral transistor region are different from each other.

First, as shown in FIG. 21A, impurities are introduced into the memory cell array region and the peripheral transistor region of the semiconductor substrate 1001 so that transistors formed in these regions may have a predetermined threshold value. Thereafter, an oxide film 1002 forming a tunnel oxide film of the memory cell transistors is formed over the surface of the semiconductor substrate. A polysilicon film 1003 doped with phosphorus as an impurity and a superposed film 1004 of a CVD (Chemical Vapor deposition) nitride film and a CVD oxide film are formed on the oxide film 1002.

Then, a resist pattern (not shown) is formed on the semiconductor substrate, and using the resist pattern as a mask the superposed film 1004 is patterned. Thereafter, the resist pattern is removed.

After that, as shown in FIG. 21B, using the patterned superposed film 1004 as a mask, the polysilicon film 1003, the gate film 1002 and the silicon substrate 1001 which are in the device isolating region forming portion are removed to form a shallow trench.

Then, as shown in FIG. 21C, an embedding insulating material, for example an LP-TEOS film, 1005 is embedded in the trenches. After that, the entire surface of the semiconductor device is flattened by using CMP (Chemical Mechanical Polishing) method or

etch-back method to polish-back or etch-back the buried insulating film 1005 to the superposed insulating film 1004. After that, a wet etching is performed to sufficiently remove the superposed insulating film 1004.

Next, as shown in FIG. 22A, a polysilicon film 1006 doped with phosphorus as an impurity is deposited over the surface of the semiconductor substrate, and then a resist pattern (not shown) is formed thereon. Using the resist pattern as a mask, the polysilicon film 1006 is patterned. In this step, slits 1007 are formed in polysilicon film 1006 on the device isolating region of the memory cell array region to divide the polysilicon film 1006 of the memory cell array region. Furthermore, in this step, the polysilicon films 1006 and 1003 in the peripheral transistor region are removed. After that, the resist pattern is removed.

Next, an ONO insulating film (a superposed film of an oxide film/a nitride film/an oxide film) 1008 is formed over the entire surface of the semiconductor substrate. Then, the ONO insulating film 1008 and the gate oxide film (a tunnel oxide film) 1002 of the peripheral transistor region are removed, while the memory cell array region is covered with a resist (not shown). After that, the resist covering the memory cell array region is removed.

When slits 1007 are formed in the memory cell

array region, the polysilicon films 1006 and 1003 in the peripheral transistor region may be left, and when the ONO insulating film 1008 and the gate oxide film (a tunnel oxide film) 1002 are removed, the polysilicon films 1006 and 1003 in the peripheral transistor region may be removed. In the foregoing state, the edges of ends of the active region in the peripheral transistor region are exposed to the outside.

Then, a state in which the memory cell array region is covered with the resist is maintained. In the foregoing state, wet etching (or an isotropic dry etching or both of the foregoing processes) is performed, as shown in FIG. 22B. Thus, the exposed edges of the ends of the active region are etched so as to be rounded.

Then, the resist covering the memory cell array region is removed, and then the gate oxide film 1009 of the peripheral transistor is formed similarly to the conventional method, as shown in FIG. 22C. Moreover, a polysilicon film into which impurities have been introduced is deposited on the overall surface of the substrate. In the memory cell array region, the polysilicon film, the ONO insulating film 1008 and the polysilicon films 1006 and 1003 are patterned so that a laminated gate structure is formed which incorporates two layers consisting of the control gate electrode 1010 and the floating gate electrode 1011 (the

polysilicon films 1006 and 1003), as shown in FIG. 22D which is viewed in a direction perpendicular to FIG. 22C. In the peripheral transistor region, the polysilicon film is patterned so that the gate electrode 1012 is formed, as shown in FIG. 22D. Then, impurities (not shown) serving as the source/drain of the transistor are selectively introduced into the surface layer of the substrate. Moreover, deposition of an interlayer insulating film, opening of a contact, wiring and deposition of a surface protective insulating film are performed. Thus, a flush EEPROM is manufactured.

FIG. 23 is an enlarged view showing the shape of an end corresponding to a portion marked with a circle drawn with a dashed line shown in FIG. 22C (that is, an end of an active region in a peripheral transistor region in which the gate oxide film has been formed after the formation of the device isolation insulating film). Reference numeral 1001 represents a semiconductor substrate, 1005 represents a device isolation insulating film, 1009 represents a gate oxide film.

As can be understood from FIG. 23, the end of the active region is rounded. Therefore, concentration of electric fields at the end of the active region experienced with the conventional structure can be prevented.

Describing the conventional manufacturing method

in relation to the seventh and eighth embodiments of the present invention, the conventional manufacturing method encounters exposure of the edge at the end of the active region during a process for removing the ONO film and the tunnel oxide film before the gate oxide film of the peripheral transistor region is formed.

As a result, according to the conventional manufacturing method, concentration of electric fields at the edge of the end of the active region takes place when the peripheral circuit transistor is operated. Thus, leak current from the peripheral circuit transistor is enlarged, causing power consumption of the device to be enlarged. The sub-threshold characteristic of the peripheral circuit transistor is made to be discontinuous with respect to the gate voltage, causing malfunction of the peripheral circuit to take place. As a result, manufacturing yield of the products have been reduced.

On the other hand, the manufacturing method according to the seventh and eighth embodiments of the present invention is structured such that (1) wet etching, isotropic dry etching, oxidizing or combination thereof with respect to the ends of the active region in the peripheral transistor region is performed to enlarge the curvature of the end of the active region or (2) bird's beaks are introduced into the ends of the active region during the process for

forming device isolation in the peripheral transistor.

Thus, falling of the gate electrode at the end of the active region can be prevented to prevent occurrence of concentration of electric field at the end of the active region of the gate electrode. Thus, leak current from the peripheral circuit transistor can be prevented, causing the sub-threshold characteristic of the peripheral transistor to be improved. Therefore, the power consumption of the product can be reduced and the manufacturing yield can be improved.

A fact is known that when the exposed edge of each end of the active region is rounded in a state in which oxidation is performed while oxygen is being supplied in a predetermined quantity, the edge can easily be oxidized as compared with flat portions.

As a substitute for the processes in each embodiment, a process may be added before formation of the gate electrode of the peripheral transistor. The process is an oxidizing process which is performed at high temperatures and in which supply of oxygen is reduced under conditions that the temperature is, for example, 1000℃ and the quantity of nitrogen is 90% and that of oxygen is 10%. In the foregoing case, the exposed edges at the ends of the active region can be rounded. When the process for forming the gate oxide film of the peripheral circuit transistor is performed by an oxidizing method with which supply is performed

with a predetermined quantity, a similar effect can be obtained. As a matter of course, the foregoing methods may be combined to obtain a similar effect.

When the gate oxide films in the memory cell array region and the peripheral transistor region are independently formed, rounding of the edges of the ends of the active region insulated and isolated by the embedded device isolating region in the peripheral transistor region is performed. Thus, the kink characteristic of the peripheral transistor having the gate electrode formed from the active region across the device isolating region can effectively be prevented.

The method of manufacturing a semiconductor apparatus according to the seventh and eighth embodiments of the present invention may be applied to a semiconductor apparatus of a type structured such that a portion of the gate insulating films is formed before formation of the device isolation and remaining gate insulating films are formed after formation of the device isolation.

By rounding the end of the active region, leak current and large power consumption in a region in which the gate voltage of the transistor is low can be prevented. Thus, the sub-threshold current characteristic is made to be continuous with respect to the gate voltage. Hence it follows that the operation of the transistor in the region in which the gate voltage is

low can stably be performed. As a result, the manufacturing yield of the products can be improved.

Therefore, when the seventh and eighth embodiments of the present invention are applied to manufacture, for example, a flush EEPROM such that the curvature of the ends of the active regions in the peripheral transistor is made to be greater than that of the end of the active region in the memory cell array region. Thus, leak current from the peripheral circuit transistor can be reduced and power consumption can be prevented.

Various embodiments of the present invention have been so far described by referring to a flush EEPROM, however the present invention is not limited thereto. For example, the peripheral circuit portion is not limited to the simple control circuit for the memory cell portion. The peripheral circuit portion may include a CPU or the like.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.